Albert Segura

Curriculum Vitae

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Personal Information

Name, Surnames	Albert Segura
Date & Place of Birth	May 2nd, 1992. Terrassa, Barcelona
Address	Jordi Girona, 1-3. Barcelona (08034), Catalunya
Citizenship	Spanish

Academic Education

September 2014 — Present
MSc and PhD in Computer Architecture, *FIB, Polytechnic University of Catalonia (UPC) BarcelonaTech*,
Research focus: Energy-Efficient GPU Architectures for Speech Recognition,
Advisors: Antonio Gonzalez, Jose-Maria Arnau.
Master's Thesis: 'Characterization of Speech Recognition Systems on GPU Architectures' (Defended in July 2016).

September 2010 — July 2014
BSc Degree in Informatics Engineering, Computer Engineering specialization, *FIB, Polytechnic University of Catalonia (UPC) BarcelonaTech*,
Final Year Project: 'Port of zeOS Operating System to an ARM architecture: Raspberry pi',
Advisor: Juan Jose Costa.

Professional Experience

September 2015 — Present
Fellowship at the ARCO group at the Computer Architecture Department, *department of AC, UPC BarcelonaTech*.
Fellowship working in research on speech recognition systems on GPU architecture platforms.

September 2014 — September 2015
Fellowship at the Programming model group at BSC, *Barcelona Supercomputing Center (BSC)*.
Fellowship working with the OmpSs programming model and the Linux Kernel to better support the Nanos++ execution runtime at the project DEEP-ER at BSC.

January 2014 — September 2014 **Fellowship at the European project Montblanc at BSC**, *Barcelona Supercomputing Center (BSC)*.
Fellowship working as a system administrator on ARM prototype platforms for HPC at the European project Montblanc at BSC.

March 2013 — January 2014 **Fellowship at the robotics department ESAII at UPC**, *department of ESAII, UPC BarcelonaTech*.
Fellowship at the robotics department of ESAII, collaborating with the Bitrack surgical project developing the hand-held to control a surgical robot.

Awards and Recognitions

2016 HiPEAC Paper Award for the paper 'An Ultra Low-Power Hardware Accelerator for Automatic Speech Recognition' (MICRO-49), HiPEAC Network of Excellence.

2014 Collaboration grant with the Computer Architecture department of UPC BarcelonaTech, Spanish government MECD AGAUR grant.

2014 Winner of the Fourth Parallel Programming Contest organized by the University of Murcia, 2014 edition.

Publications

February 2017 **'Low-Power Automatic Speech Recognition Through a Mobile GPU and a Viterbi Accelerator'**, *Reza Yazdani Aminabadi, Albert Segura, Jose-Maria Arnau, Antonio Gonzalez*, To appear in IEEE Micro Special Issue on Cognitive Architectures, February 2017.

October 2016 **'An Ultra Low-Power Hardware Accelerator for Automatic Speech Recognition'**, *Reza Yazdani Aminabadi, Albert Segura, Jose-Maria Arnau, Antonio Gonzalez*, In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (**MICRO-49**), October 2016.

Participation in Research Projects

January 2017 — Present "Arquitecturas de Sistemas de Computación Inteligentes, Ubicuos y Energéticamente Eficientes". Spanish Ministry of Economy. TIN2016-75344-R.

Conferences and other courses

July 2017 **Seminar on Modern Memory Systems by Professor Bruce Jacob (University of Maryland, USA)**, *UPC, BarcelonaTech*, Barcelona.

March 2016 **Riding on Moore's Law Workshop - RoMoL 2016**, *Barcelona Supercomputing Center (BSC)*, Barcelona.

March 2016 **Volunteer at HPCA 2016 - 22nd IEEE Symposium on High Performance Computer Architecture, 2016**, *HPCA*, Barcelona.

July 2015 **Seminar Issues in Computer Architecture and Microarchitecture for Future Computing Machine by Professor Yale Patt (University of Texas at Austin, USA)**, *UPC, BarcelonaTech*, Barcelona.

July 2014 **PUMPS 2014 - Programming and Tuning Massively Parallel Systems summer school**, *UPC, BarcelonaTech. BSC NVIDIA GPU Center of Excellence*, Barcelona.

May 2014 **Taught at PATC Course: Programming ARM based prototypes PATC Training**, *UPC, BarcelonaTech*, Barcelona.

February 2014 **MWC Intel Galileo Board Hackathon**, *MWC*, Barcelona.

February 2014 **PRACE Training: Programming Distributed Computing Platforms with COMPSs**, *UPC, BarcelonaTech*, Barcelona.

July 2013 **PUMPS 2013 - Programming and Tuning Massively Parallel Systems summer school**, *UPC, BarcelonaTech. BSC NVIDIA GPU Center of Excellence*, Barcelona.

Languages

Catalan Mother tongue

English European MECR C1.2 level *Pursuing C2 level*

Spanish Mother tongue

Skills and Competences

Programming languages

C/C++: intermediate level.
Bash, Python and Perl scripting: intermediate level.
Parallelization Models: Extensive experience with:
- CUDA (Maxwell: GTX980, Tegra X1)
- Pthreads
- OMP, OMPSS
- MPI

Assembly: Experience with x86 and Armv6 ISA, basic level.
VHDL: basic level.

Cycle-accurate simulators

GPGPUSim and GPUWattch: Extensive experience testing, extending and reviewing GPU Architecture models.

OS Development

Bare-bone OS development: Design of several simple, bare-bone OS for x86 architecture and ARM architecture: Raspberry Pi device.
Linux Kernel OS development: Extension of task core scheduling functionalities as well as its management interface.

Embedded Design

Embedded system development: Experience with Arduino (Atmel) and PIC platforms.
Eagle Software: PCB design.