REDUCING DUE-FIT OF CACHES BY EXPLOITING ACOUSTIC WAVE DETECTORS FOR ERROR RECOVERY

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IOLTS’13
Many Ways to Fail…

“Soft errors induced the highest failure rate of all other reliability mechanisms combined”

R. Baumann, IRPS’03

Cosmic Radiation -> Soft errors

Electromigration, TDDB

Qcoll < Qcrit - no error
Qcoll > Qcrit - soft error
Soft Error Rate (SER)

The Soft Error Problem

Resiliency is an enabler…
Demands the need for low-cost mainstream solutions

Challenge: Increase the degree of protection
Challenge: Reduce the protection cost

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DUE Problem

- \( \text{SER} = f(\text{SDC}, \text{DUE}) \)

Desired SDC budget per chip

Desired DUE budget per chip

Smaller caches: Error Detection

The DUE Problem

SDC-FIT is converted into DUE-FIT
These are “symptom based” solutions
Expensive for L1 cache

Cheap and simple
“Early Warning System”
Can we detect strike instead of error?
Acoustic Wave Detectors

“Setting an error detection infrastructure with low cost acoustic wave detectors” [ISCA’12]
What Is It All About?

- Error detection through particle strike detection
  - Area ~1 memory bit
  - Detection range : 5mm

- Single detector can cover area equivalent to the LLC in Nehalem Quad core (i7), 45nm
What is it all about?

Improving DUE demands
Localization accuracy of 1 bit!

System outputs
- Location of strike
- Radius in terms of CEP
- Error estimation (Area)

Localization granularity 9 bits

Unaffected bits
Quarantine bits
Estimated Location
Actual Location
Outline

- Introduction to Soft Errors
- Motivation
- Overview
- Acoustic wave detectors: Detection and Localization
- Improving DUE
- Multibit Upsets
- Results
- Conclusions
Aspects of Reliability

- Detection
- Containment
- Recovery

Minimize the latency

Find exact location of strike
Challenges

- How many detectors do I need?
  - Minimum 3 detectors
- Where should I put them?
  - Mesh configuration
- Achieve error area of 1 bit
  - Number of detectors
  - Locations of detectors
  - Number of TDOA equations
  - Sampling frequency
Detectors vs. DUE

DUE Improvement in L0 data cache

L0 data cache protected with only detectors: DUE improvement 72%
Quantification of Area [5x5 mesh]

Can we pin-point the erroneous bit out of error area bits?

- How many times error area is 2-bits, 3-bits, 4-bits and 5-bits?
Error Codes + Detectors

- Parity codes for hard errors
- Parity can be at block level or a byte level
- Can we further improve DUE by combining parity per block/parity per byte with acoustic wave detectors?
Example:

- Parity per block (Block size: 64 Bytes)
  - Both the bits in same block 😞
  - Both area bits in different blocks 😊

- We can improve the DUE of 2-bit patterns by 50%
Parity + Interleaving

- Parity per byte and bits are physically interleaved
- Degree of interleaving = 4
- DUE improvement 98%
Improvement in DUE

Error Detection Scheme

- Only Detectors: 71.85%
- Detectors + (Parity/Block): 81.89%
- Detectors + (Parity/Byte): 83.8%
- Detectors + Interleaved parity (DOI >= 4 bits): 98.18%

Legend:
- >= 6 bits
- 5 bits
- 4 bits
- 3 bits
- 2 bits
- 1bit
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Dealing with MBUs

- Temporal MBU
  - Detectors will timely detect the errors
  - No lingering single bit errors
  - Temporal MBU are treated as single bit upsets

- Spatial MBU
  - 2 and 3 bit MBU patterns
  - Little modification in the error are mask
  - Combining error codes with detectors
Dealing with MBUs

- Detectors’ accuracy is 1 bit
- Transformed into an area mask of 9 bits
- Detectors + interleaving
  - Degree of interleaving (DOI) varies
  - To cover 98% 2-bit and 3-bit MBUs the required DOI is 8
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Conclusions

- Acoustic wave detectors for particle strike detection
- Low cost and simple “*Early warning system*” for strike detection
- Accurately and timely locate the strike
- Improves the DUE by 98%
Thank you!