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PERSONAL INFORMATION

José María Arnau

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Date of birth 8 May 1985 | Nationality Spanish

SUMMARY

Distinguished researcher with over ten years of experience in Computer Architecture. Proven track record of publications in top journals and peer-reviewed conferences. Ample experience advising PhD students and teaching at University level.

WORK EXPERIENCE

September 2017 – Present

Distinguished Researcher

Universitat Politècnica de Catalunya
Barcelona, Spain

- Researching energy-efficient hardware architectures for cognitive computing
- Advising four PhD students and teaching three courses at Bachelor's and Master's level

May 2015 – August 2017

Postdoctoral Researcher

Universitat Politècnica de Catalunya
Barcelona, Spain

- Researching novel hardware architectures for machine learning workloads, considering GPGPUs, FPGAs and ASIC-based solutions
- Advising four PhD students and teaching Computer Organization course at UPC

August 2010 – April 2015

Research Assistant

Universitat Politècnica de Catalunya
Barcelona, Spain

Developing novel techniques to improve the energy-efficiency of mobile GPUs for graphics workloads. The proposed techniques substantially reduce memory bandwidth usage and avoid redundant computations of graphical applications on mobile GPUs.

August 2014 – December 2014

Architecture Intern

NVIDIA Corporation
Santa Clara, California

- Performing GPU power and performance analysis in the Applied Architecture team
- Proposing several software-level optimizations for OpenGL applications

July 2013 – September 2013

Visiting Researcher

University of Edinburgh
Edinburgh, Scotland

Performing a co-design space exploration of compiler optimizations and hardware parameters for GPGPU architectures. Using LLVM to evaluate compiler optimizations, and GPGPUSim to explore the hardware design space.

September 2008 – July 2010

Software Developer

Institute of Ceramic Technology (ITC)
Castellon, Spain

Developing several applications in C++ for scientific data visualization using OpenGL, Qt and VTK libraries.

January 2008 – June 2008

Research Assistant

Universitat Jaume I
Castellon, Spain

Developing a game engine, using C++ and OpenGL GLSL, for teaching computer graphics at the University. The engine was simple enough to be used by undergraduates, but powerful enough to render visually compelling 3D scenes.

EDUCATION AND TRAINING

March 2011 – April 2015

Ph.D. in Computer Architecture

Universitat Politècnica de Catalunya

Thesis: “Energy-Efficient Mobile GPU Systems”

Grade: Excellent Cum Laude

October 2010 – September 2011

MSc. in Computer Architecture, Networks and Systems

Universitat Politècnica de Catalunya

Thesis: “High Performance, Ultra Low Power Streaming Systems”

Grade: 9.75/10 (Award for achieving the highest overall mark)

September 2003 – June 2008

BSc. In Computer Engineering

Universitat Jaume I

Thesis: “Development of a Game Engine”

Grade: 9.64/10 (Award for achieving the highest overall mark)

PUBLICATIONS

Design and Evaluation of an Ultra Low-Power Human-Quality Speech Recognition System. Dennis Pinto, José María Arnau and Antonio González. ACM Transactions on Architecture and Code Optimization (TACO). 17, 4, Article 41 (November 2020), 19 pages. DOI:https://doi.org/10.1145/3425604

Boosting LSTM Performance Through Dynamic Precision Selection. Franyell Silfa, José María Arnau and Antonio González. In Proceedings of the 27th IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), Dec. 2020

Demystifying Power and Performance Bottlenecks in Autonomous Driving Systems. Pedro Exenberger, José María Arnau and Antonio González. In Proceedings of the IEEE International Symposium on Workload Characterization (IISWC), Oct. 2020

LAWS: Locality-AWare Scheme for Automatic Speech Recognition. Reza Yazdani, José María Arnau and Antonio González. IEEE Transactions on Computers, vol. 69, no. 8, pp. 1197-1208, 1 Aug. 2020, doi: 10.1109/TC.2020.2991002.

A Low-Power, High-Performance Speech Recognition Accelerator. Reza Yazdani, José María Arnau and Antonio González. IEEE Transactions on Computers, vol. 68, no. 12, pp. 1817-1831, 1 Dec. 2019, doi: 10.1109/TC.2019.2937075.

Neuron-Level Fuzzy Memoization in RNNs. Franyell Silfa, Gem Dot, José María Arnau and Antonio González. In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO), Oct. 2019

CGPA: Coarse-Grained Pruning of Activations for Energy-Efficient RNN Inference. Marc Riera, José María Arnau and Antonio González. IEEE Micro, vol. 39, no. 5, pp. 36-45, 1 Sept.-Oct. 2019, doi: 10.1109/MM.2019.2929742.

SCU: A GPU Stream Compaction Unit for Graph Processing. Albert Segura, José María Arnau and Antonio González. In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA), June 2019.

Performance Analysis and Optimization of Automatic Speech Recognition. Hamid Tabani, José María Arnau, Jordi Tubella and Antonio González. IEEE Transactions on Multi-Scale Computing Systems, vol. 4, no. 4, pp. 847-860, 1 Oct.-Dec. 2018, doi: 10.1109/TMSCS.2017.2739158.

E-PUR: An Energy-Efficient Processing Unit for Recurrent Neural Networks. Franyell Silfa, Gem Dot, José María Arnau and Antonio González. In Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT), Nov. 2018

The Dark Side of DNN Pruning. Reza Yazdani, Marc Riera, José María Arnau and Antonio González. In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA), June 2018

Computation Reuse in DNNs by Exploiting Input Similarity. Marc Riera, José María Arnau and Antonio González. In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA), June 2018

A Novel Register Renaming Technique for Out-of-Order Processors. Hamid Tabani, José María Arnau, Jordi Tubella and Antonio González. In Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA), Feb. 2018

UNFOLD: A Memory-Efficient Speech Recognizer Using On-The-Fly WFST Composition. Reza Yazdani, José María Arnau and Antonio González. In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO), Oct. 2017

An Ultra Low-Power Hardware Accelerator for Acoustic Scoring in Speech Recognition. Hamid Tabani, José María Arnau, Jordi Tubella and Antonio González. In Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT), Sep. 2017

Low-Power Automatic Speech Recognition Through a Mobile GPU and a Viterbi Accelerator. Reza Yazdani, Albert Segura, José María Arnau and Antonio González. IEEE Micro, vol. 37, no. 1, pp. 22-29, Jan.-Feb 2017, doi: 10.1109/MM.2017.15.

An Ultra Low-Power Hardware Accelerator for Automatic Speech Recognition. Reza Yazdani, Albert Segura, José María Arnau and Antonio González. In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO), Oct. 2016

Eliminating Redundant Fragment Shader Executions on a Mobile GPU via Hardware Memoization. José María Arnau, Joan Manuel Parcerisa and Polychronis Xekalakis. In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA), June 2014

Parallel Frame Rendering: Trading Responsiveness for Energy on a Mobile GPU. José María Arnau, Joan Manuel Parcerisa and Polychronis Xekalakis. In Proceedings of the IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (PACT), Sept. 2013

TEAPOT: A Toolset for Evaluating Performance, Power and Image Quality on Mobile Graphics Systems. José María Arnau, Joan Manuel Parcerisa and Polychronis Xekalakis. In Proceedings of the ACM International Conference on Supercomputing (ICS), June 2013

Boosting Mobile GPU Performance with a Decoupled Access/Execute Fragment Processor. José María Arnau, Joan-Manuel Parcerisa and Polychronis Xekalakis. In Proceedings of the IEEE/ACM International Symposium on Computer Architecture (ISCA), June 2012

Study of the Pressing Operation of Large-sized Tiles Using X-ray Absorption. J.L. Amoros, G. Mallol, D. Llorens, J. Boix, J.M. Arnau, C.Feliu, J.A. Cerisuelo and J.J. Gargallo. Journal of the Spanish Ceramic and Glass Society, vol. 49, no. 4, pp. 279-288, 2010

Apparent Density Measurement of the Ceramic Tiles in a Quick, Harmless and Non-destructive Way. G. Mallol, D. Llorens, J. Boix, M. Aguilella, L. Foucard and J.M. Arnau. Journal of the Spanish Ceramic and Glass Society, vol. 49, no. 6, pp. 393-398, 2010

TEACHING

September 2017 – January 2020

Computer Organization

Universitat Politècnica de Catalunya

BSc. Degree on Computer Engineering

224 hours of theory sessions and 36 hours of lab sessions

September 2019 – January 2020

Processor Design

Universitat Politècnica de Catalunya

MSc. in Innovation and Research in Informatics

28 hours of theory sessions

February 2020 – July 2020

Nanoelectronic Circuit Design

Universitat Politècnica de Catalunya

MSc. in Innovation and Research in Informatics

28 hours of theory sessions and 28 hours of lab sessions

PHD ADVISING

July 2020 – Present

Mojtaba Abaie

Thesis title: “GPGPU Architectures for Cognitive Computing”

January 2020 – Present

Pedro Exenberger

Thesis title: “An Energy-Efficient Accelerator for Self-Driving Cars”

September 2019 – Present

Raul Taranco

Thesis title: “Low-power, High-performance Architectures for Camera-based Autonomous Driving”

April 2018 – Present

Daniel Pinto

Thesis title: “Energy-Efficient Architectures for Human-Quality Speech Recognition Systems”

September 2016 – February 2021

Albert Segura

Thesis title: “High-Performance and Energy-Efficient Irregular Graph Processing on GPU architectures”

Grade: Excellent Cum Laude

September 2016 – January 2021

Franyell Silfa

Thesis title: “Energy-Efficient Architectures for Recurrent Neural Networks”

Grade: Excellent Cum Laude

September 2015 – October 2020

Marc Riera

Thesis title: “Low-Power Accelerators for Cognitive Computing”

Grade: Excellent Cum Laude

September 2015 – July 2019

Reza Yazdani

Thesis title: “Ultra Low-Power, High Performance Accelerator for Speech Recognition”

Grade: Excellent Cum Laude

LANGUAGES

Spanish: Native speaker

Catalan: Native speaker

English: Fluent

AWARDS AND HONORS

2012 **Intel Doctoral Student Honor Programme**
$35000 awarded by Intel Corporation for performing outstanding research in the area of Computer Architecture

2011 **FI Research Grant**
Funding from the Catalan Government for a three year Ph.D.

2011 **Best Student Graduating in Master's Degree on Computer Architecture**
Awarded by the Faculty of Informatics at the Universitat Politècnica de Catalunya

2010 **Second Best Student Graduating in Computer Engineering in Spain**
Awarded by the Spanish Government

2009 **Best Student Graduating in the Valencian Community**
Awarded by the Valencian Government

2008 **Best Student Graduating in Computer Engineering**
Awarded by the Universitat Jaume I

2008 **Best Student Graduating in Computer Engineering**
Awarded by the School of Technology and Experimental Sciences of Castellon

2007 **Research Collaboration Grant from the Spanish Ministry of Education**
Funding for a six-month research collaboration in the Computer Graphics Group at the Universitat Jaume I of Castellon

HiPEAC Paper Award
Awarded by the European Network on High-performance Embedded Architecture and Compilation for publishing papers in top Computer Architecture conferences. I have received the award seven times for my papers published in HPCA, ISCA and MICRO.

PARTICIPATION IN RESEARCH PROJECTS

September 2019 – Preset
CoCoUnit: An Energy-Efficient Processing Unit for Cognitive Computing
Researcher staff. Funded by European Research Council.

January 2017 – December 2020
Architectures for Intelligent, Ubiquitous and Energy-Efficient Computing Systems
Researcher staff. Funded by Spanish Ministry of Economy. TIN2016-75344-R.

January 2014 – December 2016
Microarchitectures and Compilers for Future Processors III
Researcher staff. Funded by Spanish Ministry of Economy. TIN2013-44375.

January 2011 – December 2013
Microarchitectures and Compilers for Future Processors II
Researcher staff. Funded by Spanish Ministry of Science and Technology. TIN2010-18368.

ORGANIZATION OF CONFERENCES

September 2015 – March 2016
Publications Chair
IEEE/ACM International Symposium on High Performance Computer Architecture