DRAM-based On-Chip Cache Architectures to Combat Process Variations

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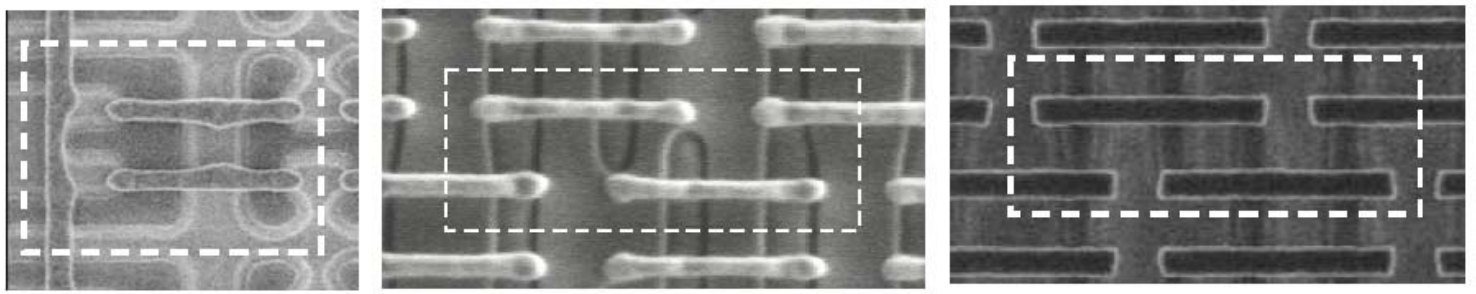
Overview

- **Impact of process variations (PV) is becoming increasingly important.**
- **Traditional 6T-based SRAM structures are especially sensitive to PV.**
- **We propose to replace SRAM by DRAM in L1-data cache.**

Using architecture solutions to solve the PV problem in circuit and device !!

PV Impact on 6T SRAMs



90nm – tall
1.0 μm²

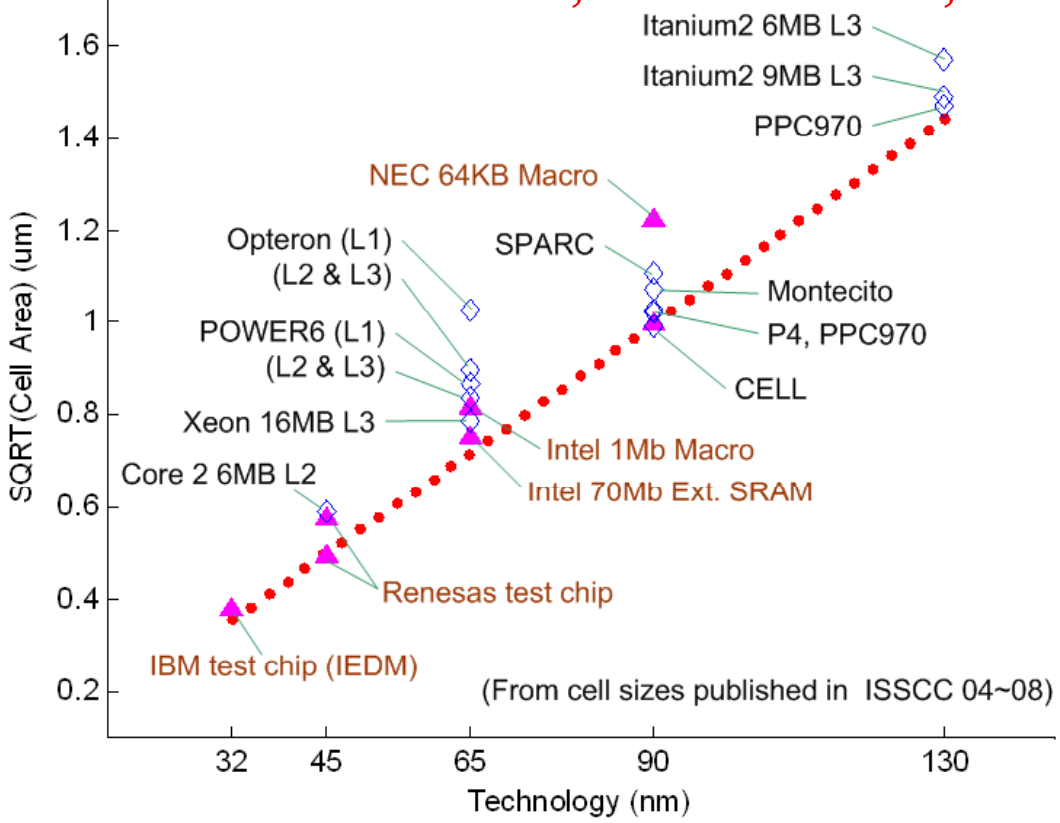
65nm – wide
0.57 μm²

45nm – wide
w/ patterning enhancement 0.346 μm²

Intel SRAM cell size scaling (IEDM'07)

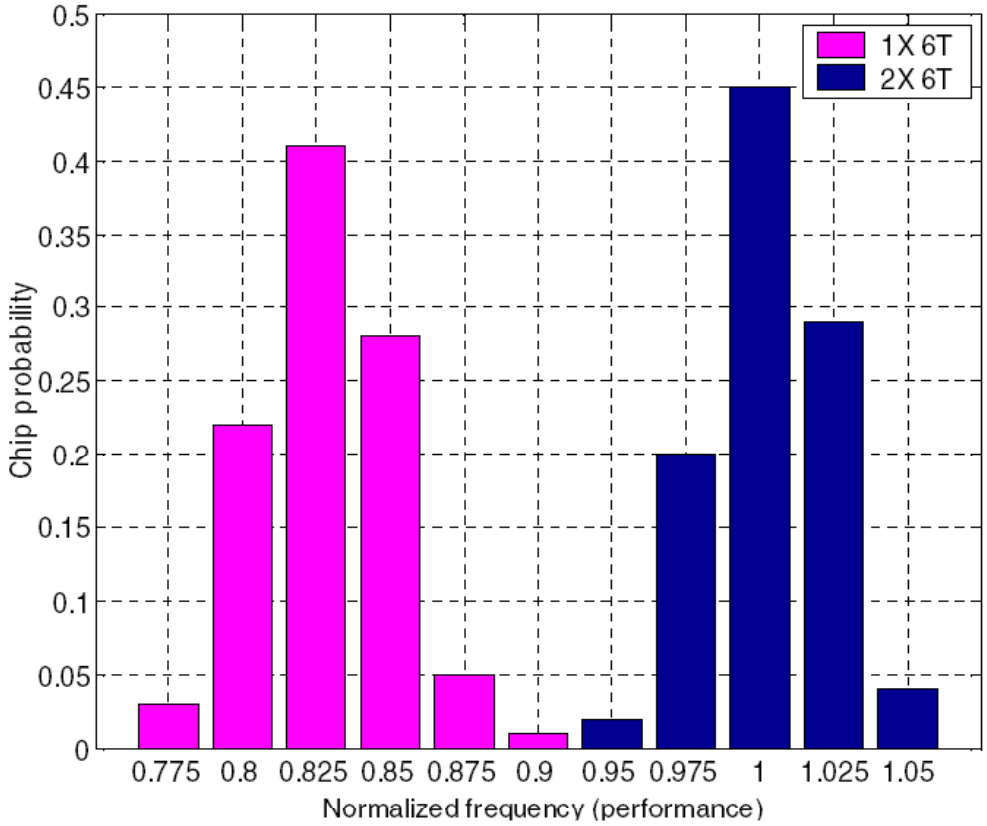
Deviation from Ideal Scaling: 90nm-> 0%, 65nm->14%, 45nm->39%

Equal Die Size Cache: 90nm 1MB, 65nm 1.75MB, 45nm 2.89MB



6T SRAM Performance

- **Process variation → access time variations**
  - → **Limits frequency across entire system under typical variations**

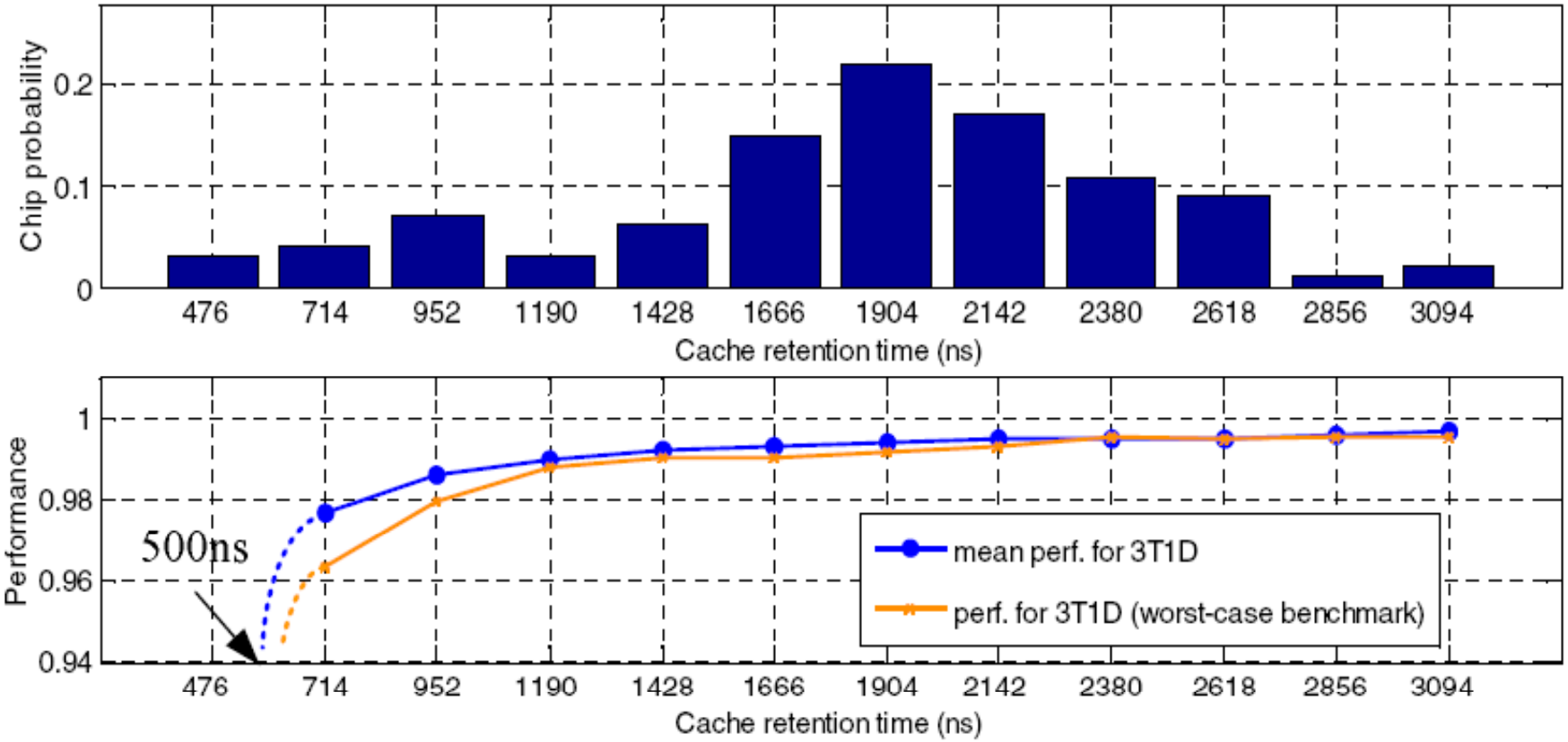


  - → **Large Performance loss under severe variations (64% line failure)**

3T1D w/ Typical Variations

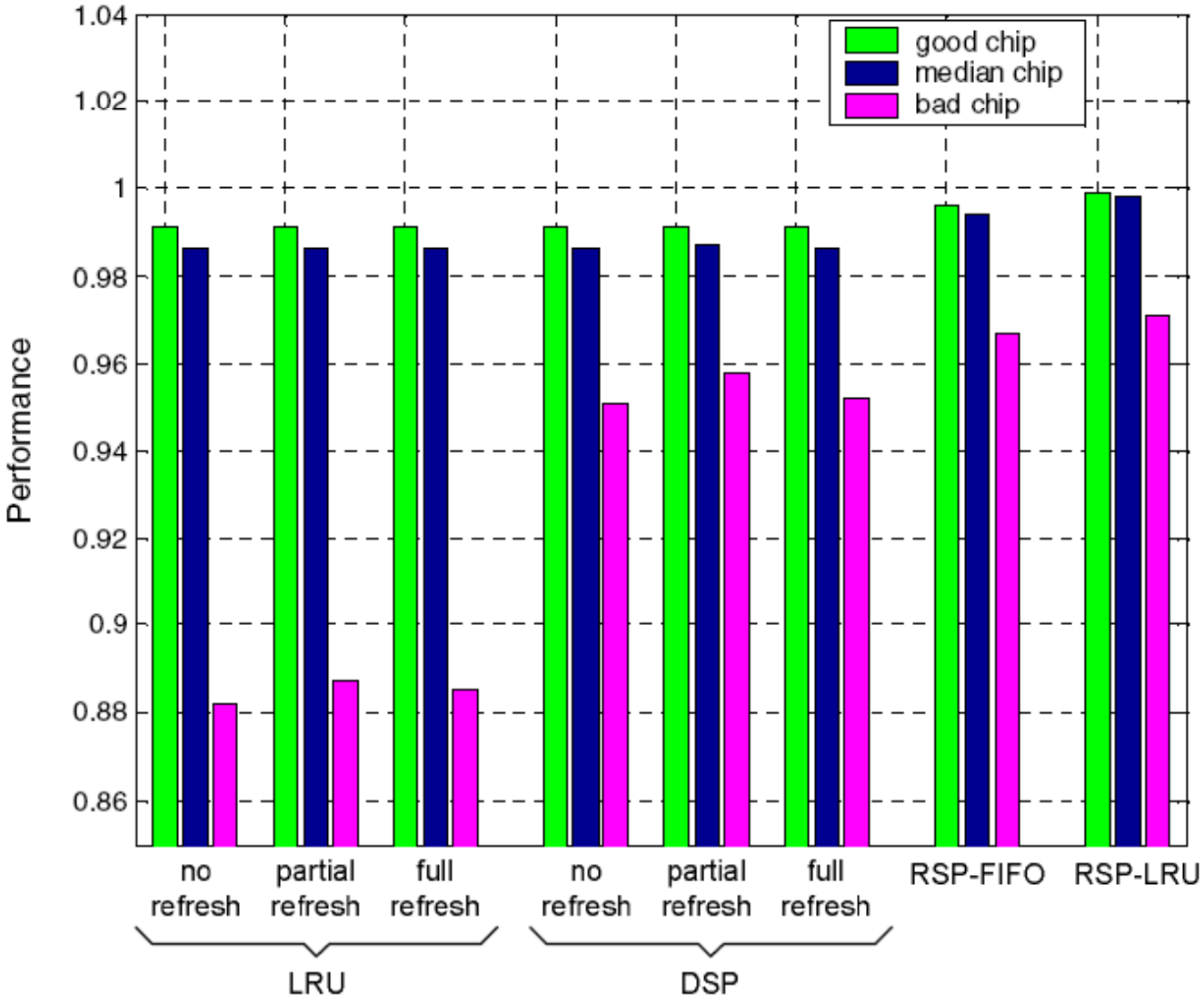
$\sigma L/L_{nominal}$ (WID)	5%
$\sigma V_{th}/V_{th}$ (WID)	10%
$\sigma L/L_{nominal}$ (D2D)	5%

- **Process variation → retention time variations**
  - → **Small performance loss**



3T1D w/ Severe Variations

$\sigma L/L_{nominal}$ (WID)	7%
$\sigma V_{th}/V_{th}$ (WID)	15%
$\sigma L/L_{nominal}$ (D2D)	5%



2-way approach:

1) Line refresh
   No, partial, full

2) Smart line placement
   DSP: Dead Sensitive Policy
   RSP: Refresh Sensitive Policy

Even under sever variations, ALL chips perform within 5% of the optimal!!